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**1 Low density parity check (LDPC) codes for optical data storage**

*Bhagavatula, V.; Hongwei Song; Jingfeng Liu;*  
Optical Memory and Optical Data Storage Topical Meeting, 2002. International Symposium on , 7-11 July 2002

Pages:371 - 373

[\[Abstract\]](#) [\[PDF Full-Text \(258 KB\)\]](#) IEEE CNF

**2 Differential space-time turbo codes**

*Schlegel, C.; Grant, A.;*  
Information Theory, IEEE Transactions on , Volume: 49 , Issue: 9 , Sept. 2003  
Pages:2298 - 2306

[\[Abstract\]](#) [\[PDF Full-Text \(398 KB\)\]](#) IEEE JNL

**3 Binary intersymbol interference channels: Gallager codes, density evolution, and code performance bounds**

*Kavcic, A.; Xiao Ma; Mitzenmacher, M.;*  
Information Theory, IEEE Transactions on , Volume: 49 , Issue: 7 , July 2003  
Pages:1636 - 1652

[\[Abstract\]](#) [\[PDF Full-Text \(1058 KB\)\]](#) IEEE JNL

**4 On-chip error correcting techniques for new-generation flash memory**

*Gregori, S.; Cabrini, A.; Khouri, O.; Torelli, G.;*  
Proceedings of the IEEE , Volume: 91 , Issue: 4 , April 2003  
Pages:602 - 616

[\[Abstract\]](#) [\[PDF Full-Text \(600 KB\)\]](#) IEEE JNL

**5 Synonym hit RAM - a 500-MHz CMOS SRAM macro with 576-bit parallel comparison and parity check functions**

Suzuki, T.; Higeta, K.; Fujimura, Y.; Ando, K.; Nambu, H.; Yamagata, R.; Hoia, A.; Yamaguchi, K.;

Solid-State Circuits, IEEE Journal of , Volume: 35 , Issue: 2 , Feb. 2000

Pages:163 - 174

[Abstract] [PDF Full-Text (280 KB)] IEEE JNL

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**6 Cycle-slip-detector-aided iterative timing recovery algorithm**

Xiaowei Jin; Kavcic, A.;

Magnetics Conference, 2002. INTERMAG Europe 2002. Digest of Technical Papers , 2002 IEEE International , 28 April-2 May 2002

Pages:BR2

[Abstract] [PDF Full-Text (225 KB)] IEEE CNF

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**7 Design and implementation of error detection and correction circuit multilevel memory protection**

Polianskikh, B.; Zilic, Z.;

Multiple-Valued Logic, 2002. ISMVL 2002. Proceedings 32nd IEEE International Symposium on , 15-18 May 2002

Pages:89 - 95

[Abstract] [PDF Full-Text (315 KB)] IEEE CNF

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**8 Synonym hit RAM; a 500 MHz 1.5 ns CMOS SRAM macro with 576 bits parallel comparison and parity check functions**

Suzuki, T.; Higeta, K.; Fujimura, Y.; Nambu, H.; Yamagata, R.; Yamaguchi, S.; Solid-State Circuits Conference, 1998. Digest of Technical Papers. 45th ISSCC 1998 IEEE International , 5-7 Feb. 1998

Pages:348 - 349

[Abstract] [PDF Full-Text (596 KB)] IEEE CNF

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**9 Autonomous Line Scanning for SPC Telephone Switching Systems**

Shrivastava, A.; Ramanadhan, P.; Shah, A.; Jamadagni, H.;

Communications, IEEE Transactions on [legacy, pre - 1988] , Volume: 26 , Issue: 3 , Mar 1978

Pages:368 - 373

[Abstract] [PDF Full-Text (656 KB)] IEEE JNL

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**10 Optimum error detection codes for noiseless decision feedback**

Jacobs, I.;

Information Theory, IEEE Transactions on , Volume: 8 , Issue: 6 , Oct 1962

Pages:359 - 371

[Abstract] [PDF Full-Text (1872 KB)] IEEE JNL

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**11 Optimized low-density parity-check codes for partial response channels**

Varnica, N.; Kavcic, A.;

Communications Letters, IEEE , Volume: 7 , Issue: 4 , April 2003

Pages:168 - 170

[\[Abstract\]](#) [\[PDF Full-Text \(300 KB\)\]](#) [IEEE JNL](#)

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**12 Time-varying periodic convolutional codes with low-density parity-check matrix**

*Jimenez Felstrom, A.; Zigangirov, K.S.;*

Information Theory, IEEE Transactions on , Volume: 45 , Issue: 6 , Sept. 199  
Pages:2181 - 2191

[\[Abstract\]](#) [\[PDF Full-Text \(444 KB\)\]](#) [IEEE JNL](#)

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**13 Implementation of an environment of symbolic model checking based on the TDGs**

*Ayadi, S.; Lakhnech, Y.; Robbana, R.;*

Computer Systems and Applications, 2003. Book of Abstracts. ACS/IEEE International Conference on , 14-18 July 2003  
Pages:97

[\[Abstract\]](#) [\[PDF Full-Text \(172 KB\)\]](#) [IEEE CNF](#)

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**14 Symbolic model checking for real time systems using difference type decision graphs**

*Ayadi, S.; Robbana, R.;*

Computer Systems and Applications, 2003. Book of Abstracts. ACS/IEEE International Conference on , 14-18 July 2003  
Pages:72

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**15 Hybrid analysis of three-dimensional structures by the method of I using novel nonequidistant discretization**

*Greda, L.A.; Pregla, R.;*

Microwave Symposium Digest, 2002 IEEE MTT-S International , Volume: 3 , June 2002  
Pages:1877 - 1880

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